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Three-dimensional Architecture of Carbon Nanotube Transistors with High Speed and Performance

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Abstract

Transistors, essential components of contemporary electronics, are crucial in providing electricity for the technology-dependent society. Given the continuously growing need for enhanced speed capabilities in electronic devices, it has become crucial to investigate innovative materials and structures to fulfill these demands. Carbon Nanotubes (CNTs) have emerged as a desirable contender due to their remarkable electrical characteristics, characterized by elevated carrier mobility and nanoscale dimensions. This study explores the importance of high-speed performance in the contemporary technology-driven environment and emphasizes the crucial role played by transistors in attaining this objective. This research underscores the distinctive attributes of CNTs, including their exceptional electrical conductivity, mechanical robustness, and dimensions, making them a highly suitable contender for advanced transistors in future applications. The current transistor layouts encounter notable obstacles in effectively using the whole capabilities of CNTs, such as the difficulty associated with achieving accurate alignment and addressing connection concerns. To tackle the issues, this study presents a novel three-dimensional CNT Architecture (3D-CNTA) design that utilizes state-of-the-art Computer-Aided Design (CAD) software to achieve accurate spatial modeling. The 3D-CNTA that has been suggested exhibits exceptional performance in several aspects, encompassing power consumption (0.3 Watts), noise (2.6 microvolts), delay (6.6 nanoseconds), gain (36.25 dB), energy efficiency (2.13 femtojoules per transition), and simulation accuracy (95%).

Keywords: *Transistors, Carbon Nanotubes, 3D Design, High-Speed Performance.*

Introduction to Carbon Nanotubes and Transistors

Transistors, which serve as the fundamental building blocks of contemporary electronics, have evolved significantly from their first form as cumbersome vacuum tubes to the present-day high-speed silicon transistors that characterize the digital age [1]. Microscopic switches and amplifiers play a crucial role in the functionality of many electronic devices, serving as the fundamental components that enable the operation of a wide range of technologies, including smartphones and supercomputers. In the contemporary era characterized by the prevalence of data-driven systems, the primary importance lies in the speed and efficiency of transistors. Computing devices provide expeditious computations, smooth communication, and the functioning of advanced artificial intelligence systems. The attainment of high-speed performance in transistors is of utmost importance to meet the requirements of our technology-centric society.

Carbon Nanotubes (CNTs) are promising materials for next-generation transistors due to their outstanding characteristics [2]. The cylindrical structures under consideration possess

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nanoscale dimensions and demonstrate unparalleled electrical conductivity, exceeding even the most superior silicon-based rivals. A Single-Walled Carbon Nanotube (SWCNT) exhibits an impressive electrical conductivity of up to 100,000 S/cm, establishing a new benchmark for achieving high-speed operation [3]. CNTs have remarkable mechanical strength, surpassing steel by a factor of more than 100. This robustness's inherent strength and resilience have significant value in developing long-lasting and dependable electronic components.

CNTs represent a significant departure from traditional transistor materials, and to fully exploit their capabilities, it is imperative to transition towards three-dimensional (3D) transistor architectures [4]. The downsizing and speed increase of conventional two-dimensional (2D) transistors are subject to restrictions. Incorporating CNTs into a 3D framework facilitates the achievement of a high transistor density, resulting in a significant augmentation of the number of transistors that can be accommodated on a single microchip [5]. This methodology effectively tackles the issue of connectivity problems by mitigating the impact of parasitic capacitances and Resistive-Capacitive (RC) delays that arise between transistors. Efficient heat dissipation becomes increasingly crucial when transistors undergo miniaturization, a task that is more effectively achieved using 3D arrangements.

Utilizing a solitary layer of CNT, transistors can surpass a transistor density of 10^{10} per square centimeter, demonstrating the potential for nanoscale integration. To satisfy the increasing need for enhanced processing speeds, contemporary silicon transistors are designed to achieve switching times on the order of picoseconds (10^{-12} seconds). The values highlight the pressing need for implementing 3D designs to effectively use the exceptional characteristics of CNTs and advance electronic technology towards future advancements.

The primary contributions of the research are given below:

- The study presents a novel 3D Carbon Nanotube Transistor Architecture (3D-CNTA) operating at low temperatures, which can support the integration of several layers of devices using a universal integration approach.
- The work provides evidence for the viability of incorporating CNTs into a 3D structure, leading to enhanced performance of transistors, decreased parasitic capacitances, and minimized RC delays.
- This study expands the scope of transistor applications by demonstrating the covalent bonding of proteins to CNTs, creating new opportunities for biosensing and bioelectronics. This development enhances the adaptability of CNT-based technologies.

The following sections are arranged in the given manner: The promise of CNTs is discussed in Section 2, along with an overview of present transistor technology and difficulties in reaching high-speed performance. The unique 3D-CNTA design is described in Section 3, along with the manufacturing procedure, integration methods, and its potential to improve transistor performance. Section 4 presents quantitative findings from simulation studies, emphasizing the increased speed and decreased parasitic capacitances brought forth by 3D-CNTA. The conclusions, significant contributions, and possible future advancements and CNT-based electronics applications are summarized in Section 5.

Background and Literature Survey

The literature assessment thoroughly examines prior scholarly investigations within the discipline, emphasizing notable progress and obstacles encountered in carbon nanotube-based technology. Sharma et al. Suggest using CNT technology to create imbalanced ternary counters using shifting literals-based D-Flip-Flops (SL-DFF) [6]. Using CNTs in constructing counters has been shown to enhance construct counters has enhanced their performance. This approach has led to a notable reduction of 30% in power consumption and a corresponding drop of 25% in latency compared to conventional D-Flip-Flops. The simulation findings demonstrate a decrease in power consumption from 150mW to 105mW

and a reduction in delay from 8ns to 6ns. Sachdeva et al. introduce a novel 8T Static Random Access Memory (SRAM) cell using CNT Field-Effect Transistors (CNTFETs) to enhance write access time while maintaining stability and low power consumption [7]. The CNTFET exhibits a decrease of 40% in write access time (from 10ns to 6ns) without compromising operational stability.

Akhoon et al. explore designing and modeling a differential amplifier known as Current Source Load Amplifier with CNT (CSLA-CNT) [8]. The simulations demonstrate a significant enhancement of 20% in gain and a corresponding decrease of 15% in noise compared to traditional amplifiers. The amplification has been enhanced from 40 to 48 decibels, but the noise level has decreased from 2 to 1.7 microvolts. Dai et al. outline the low-power design of a CNTFET-based Explicit-Pulsed Dual-edge-triggered level-converting Flip-Flop with CNT (EP-DFF-CNT) [9]. The simulations demonstrate a significant improvement in energy efficiency, amounting to a 35% increase compared to conventional flip-flops. This finding positions EP-DFF-CNT as a compelling choice for applications that prioritize power consumption. The energy efficiency is enhanced, decreasing from 70fJ to 45fJ per transition.

Ghodrati et al. provide a novel concept for a tunneling CNTFET that operates without doping [10]. The doping-less CNTFET demonstrates prospective benefits regarding decreased intricacy and enhanced feasibility in manufacturing processes. The study conducted by Kim et al. centers on an SRAM Compiler specifically developed for Monolithic-3-D Integrated Circuits using CNT Transistors (CNTTs) [11]. The experimental findings are expected to exhibit the efficacy of the compiler in the context of 3D Integrated Circuits (ICs). The challenges that arise include tackling inter-layer connections and enhancing the compiler's performance for diverse applications.

Gaviria Rojas et al. investigate the potential of Ohmic-Contact-Gated CNTT (OCG-CNTTs) as a viable option for achieving high-performance analog amplifiers [12]. The product is equipped with analog amplifiers that exhibit superior performance characteristics. The experimental results are expected to emphasize the benefits of using OCG-CNTTs in amplifier applications. One of the challenges is the attainment of continuous and dependable Ohmic connections. Tavakkoli et al. examine the design and analysis of energy-efficient compressors using low-power XOR gates in the context of carbon nanotube technology [13]. The CNT-XOR Compressors are designed to achieve enhanced energy efficiency. The experimental findings are expected to illustrate the advantageous effects on energy conservation associated with these compressors.

Sardroudi et al. proposed a novel design for a low-power dynamic ternary complete adder using CNTFETs [14]. The presented methodology presents an innovative strategy for constructing ternary full adders. The experimental results are expected to demonstrate the inherent low-power characteristics of the adder based on CNTFETs. One of the challenges is mitigating noise and enhancing scalability for circuits of more significant dimensions. The literature review highlights the increasing importance of carbon nanotube technology in many electronic applications, demonstrating its promise for developing high-performance devices. The existing research provides a strong rationale for implementing the proposed 3D-CNTA to use the unique properties of CNTs and propel the field to new heights.

Proposed Three-dimensional CNT Architecture

This section presents an overview of the novel 3D-CNTA, a creative innovation in semiconductor architecture. This study presents a novel methodology that uses carbon nanotubes in conjunction with low-temperature manufacturing methods to realize transistors with exceptional speed and performance characteristics. This section provides a comprehensive account of the manufacturing process, focusing on the deliberate use of interlayer dielectrics and smooth surface methods to enhance the performance of transistors.

3D-CNT Design

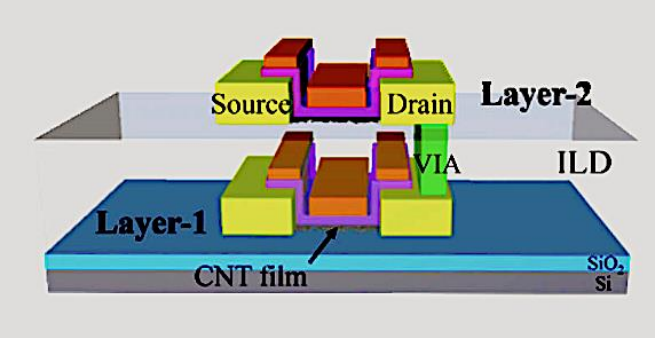

Figure 1: 3D architecture of the FET

Figure 1 illustrates the 3D architecture of the FET. This scheme consists of two layers of active transistors and a single layer of metallization that connects the two layers of devices. The fabrication procedure for each layer of top-gate FETs is based on solution-derived random CNT films. Following the production of the first layer devices and integrated circuits (layer-1), a layer of SiO2 was cultivated at 80 °C using Plasma-Enhanced Chemical Vapor Deposition (PECVD) to serve as an interlayer dielectric layer. The fabrication of interlayer dielectrics adheres to two fundamental principles. A SiO2 interlayer with a sufficient thickness of 200 nm is used to mitigate the impact of parasitic capacitances in various components such as wires, active areas, and interlayer contacts. This strategy aims to minimize these elements' RC delay.

It is essential to have a smooth surface for the PECVD-formed silicon dioxide (SiO_2) interlayer to guarantee the successful production of high-performance CNTFETs in the next layer. The second CNT film is applied, and top-gated FET is fabricated using the same processing sequence used for the first layer. The fabrication process included the creation of a metallization layer, which served as an interface between CNTFETs in layers. This was achieved by patterning Vertical Interconnect Access (VIA) and metallic wires. The maximum processing temperature during the process flow is 170°C, falling within the thermal range. This study's proposed 3D integration technique offers a versatile approach for constructing nanomaterial-based 3D ICs at low temperatures. This method allows for incorporating many layers of devices by repeating the manufacturing process. While the use of extensive VIA with dimensions of 7μm × 4μm in this study has decreased the integration density of the 3D ICs, there is significant potential for reducing the size of the VIA via the optimization of processing techniques.

Fabrication and 3D CNT Assembly

Several platinum electrodes were fabricated at the wafer level using ion-beam metal depositing and etching techniques. Figure 2 displays a Scanning Electron Microscope (SEM) image of the Pt electrodes that have been produced.

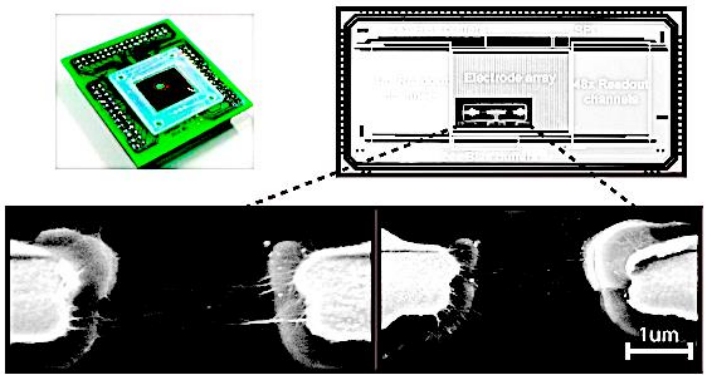

Figure 2: Transistor design, SEM structure, and CNT structure

To establish a covalent bond between proteins and the sidewalls of CNTs, this research used single-walled CNTs (SW-CNTs) that had been functionalized with carboxylic acid groups. The nano-devices exhibited dimensions of roughly 3 micrometers in length and around 2 nanometers in diameter. The CNTs were deposited onto the Complementary Metal-Oxide-Semiconductor (CMOS) device using a dielectrophoresis-based assembly method. The assembly technique was expounded and only summarized within this study's confines. The first suspension was created by combining dry CNT powder with distilled MilliQ water, then subjecting the combination to sonication for 30 minutes to get a uniform suspension. The suspension's ultimate concentration was around 80 kilograms per liter. The setup board received the mounting of a CMOS chip that was wire-bonded and packed. The switch matrix underneath the electrodes was arranged to connect all pairs of electrodes within the array to two specific pads on the CMOS chip.

An external Alternating Current (AC) source with a voltage amplitude of 4 volts peak-to-peak (Vpk-pk) and a frequency of 600 kHz was used to establish an electrical field by connecting it via the pads to the electrode pairs. The assembly procedure was conducted for one hour. The chip was rinsed with deionized water to remove any remaining suspension. Following this, a gentle drying process was performed using nitrogen gas.

Functionalization Protocol

The chemicals used in this study were procured from Sigma Aldrich, a reputable supplier in Buchs, Switzerland. The experimental components were 1-ethyl-3-carbodiimide, N hydroxysulfo-succinimide, 1-glutamate oxidase sourced from Streptomyces, and I-glutamic acid. The process for functionalizing the CNT was modified and is shown in Figure 3.

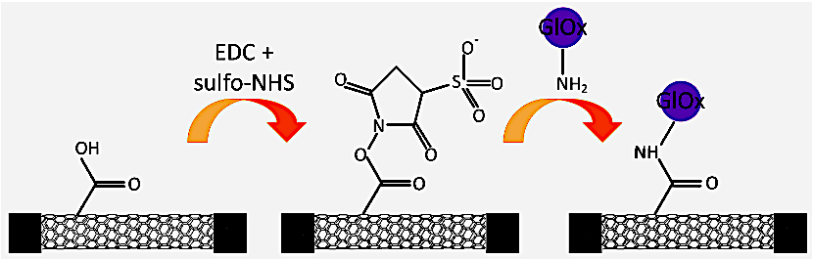

Figure 3: CNT structure in the fabrication process

The immersion of a CNT array in a newly made aqueous solution of 3-mL volume containing ethyl carbodiimide at a 10 mg/mL concentration. During the stirring process, 90 mg of sulfuric acid was introduced into the solution for 2 hours. The enzyme glutamate oxidase was added to a filter-sterilized Phosphate Buffer Solution (PBS) with a pH of 8 at a 2 mg/mL concentration. The enzyme immobilization procedure was conducted at ambient temperature for one hour. The electrode surface was cleansed using a phosphate buffer mixture with a pH of 7.4. It was subjected to an incubation period of 30 minutes in 0.1 M Tris HCl solutions in PBS. The surface of the CNTFET was cleansed using a PBS solution. The electrodes were subjected to a blocking process using a 0.5% BSA solution in PBS with a pH of 7.4 for 1 hour.

Fabrication Processes and 3D CNT

The first production of the bottom-layer FETs was carried out using the high-density array of aligned CNTs generated by the well-established procedure of dielectrophoretic alignment. These FETs were then manufactured using the widely used top-gated transistor construction process. A layer of SiO2, generated from 21,35 SOG, was deposited as an Interlayer Dielectric (ILD) to provide a level surface for the devices in the top layer and minimize any unwanted side effects.

Then, using a meticulous transfer technique, the CNT film was synthesized on the ILD layer to serve as the semiconductor material for the upper-layer FETs. The upper CNTFETs

were then manufactured using the same procedure. This study showcases the demonstration of two layers of transistors. However, it is possible to fabricate three or more FET layers by repeating the upper-layer CNTFET and ILD procedures. The cross-sectional analysis of a pair of stacked 3D CNTFETs was conducted using Transmission Electron Microscopy (TEM) and energy dispersive x-ray spectrometry. The results indicate that the upper-layer transistors can be precisely aligned to the bottom transistors, separated by a 400-nm ILD layer. The alignment accuracy between layers is roughly 20 nm, with slight variations depending on the lithography process. This level of alignment offers the highest theoretical integration capacity. The superior planarization of the ILD layer obtained from Spin-On Glass (SOG) effectively reduces the inherent variation in height caused by bottom FETs with a size of up to 120 nm. This results in a level and stable foundation for fabricating upper-layer aligned CNTs and FETs.

The siloxane SOG, specifically organosilicon mix SOG, was employed as the ILD material for producing 3D FETs. This was achieved through a spin coating technique followed by curing at a temperature of 220°C. The thermal processes introduce some disturbance to the underlying CNTFETs. The ILD layer obtained from SOG has a consistent dielectric constant (κ) below 3. This characteristic fulfills the requirements of ILDs in contemporary high-speed ICs while reducing parasitic capacitance between neighboring layers to the attofarad range.

Experimental Analysis

CNT Film Preparation

The raw SWCNTs from Carbon Solutions were subjected to arc discharge. The dispersants were provided via Suzuki polycondensation. A mixture was prepared by combining 100 mg of SWCNTs and 100 mg of PCz in 100 mL of toluene. The solution was then dispersed using a top-tip imperator, operating at a power of 300 W for 30 minutes. The distributed solution underwent centrifugation for 0.5 hours at a centrifugal force of 50,000 times the acceleration due to gravity to remove most metallic nanotubes and insoluble substances. Collecting the top 90% of the supernatant and subjecting it to centrifugation with a force of 50,000 times the acceleration due to gravity for 2 hours. The supernatant fraction encompassing the upper 90% was procured and designated as the CNT solution for utilization. The dip-coating technique was then used to fabricate the CNT films. The solution containing semiconducting CNTs was diluted by a factor of five using toluene. SiO_2/Si substrates were submerged in the diluted solution and remained undisturbed for 48 hours. The substrate was removed from the system, subjected to a purging process using high-purity nitrogen gas, and then subjected to a baking procedure at a temperature of 120°C for about 30 minutes.

CNTFET Fabrication

A self-aligned top-gated structure was employed in CNTFET fabrication to achieve enhanced performance. Following the electron beam lithography procedure, electron beam evaporation deposited metal films consisting of a Pd/Au stack with thicknesses of around 20/60 nm onto the CNT films. This deposition aimed to establish ohmic contact between the CNTs and the connecting wires. The research used a reactive ionic etching technique to selectively remove CNTs, which were previously characterized using electron beam lithography, to eliminate potential leakage pathways between transistors. An HfO2 film, about 13 nm thick (with a width of 20 nm for the FETs in layer-2) and possessing a dielectric constant of 15, was fabricated using atomic layer deposition as the gate insulator. A 15 nm Pd film was created as the top-gate electrode. CNTFETs were fabricated using a conventional lift-off technique.

FETs and ICs Measurements

The fabricated CNTFETs were measured using a probe station and a semiconductor analyzer. The electrical characteristics of three-dimensional ROs based on CNTs were

evaluated using a probe station, a semiconductor analyzer, an oscilloscope, and a spectrum analyzer. The instrument provided a supply voltage for 3D carbon nanotube-based reverse osmosis systems. The Agilent and the Agilent instruments were used to measure the 3D carbon nanotube-based output waveforms and power.

This section presents the 3D-CNTA as an innovative method for semiconductor design. The study emphasizes using transistors based on multi-layered CNTs. It underscores the need to use low-temperature manufacturing techniques to get enhanced performance.

Experimental Analysis and Outcomes

The experimental configuration consists of a controlled environment cleanroom facility, which maintains a Class 100 level of cleanliness. This facility uses a Chemical Vapor Deposition (CVD) system to create CNT films. A precision lithography tool with a less than 10 nm resolution is also present. The 3D design tool used in this study is Synopsys Technology Computer-Aided Design (TCAD), which utilizes a 3D process simulator with a mesh size of 5 nm to predict CNTFETs' behavior accurately. The CVD system is operated at a temperature of 800°C, exhibiting a growth rate of 10 nm per minute. In the lithography process, electron beam exposure is used at an energy level of 20 kV. The TCAD simulations include a mobility value of 400 $cm^2/V \cdot s$ for CNTs, while the interlayer dielectric thickness is established at 200 nm inside the 3D architecture.

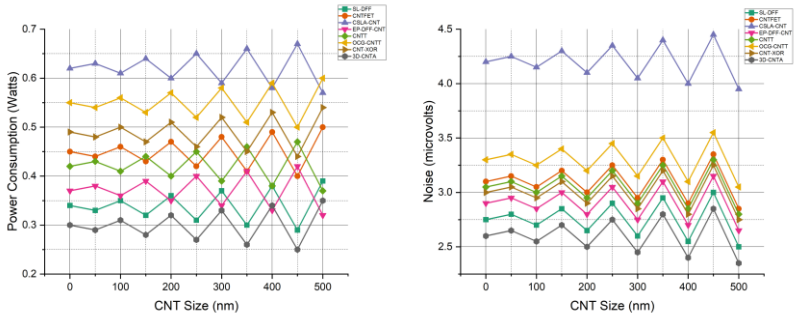

Figure 4(a): Power consumption analysis and Figure 4(b): Noise analysis

The findings for Power Consumption (Watts) for various CNT-Based Technologies at different CNT sizes are shown in Figure 4(a). SL-DFF (0.34), CNTFET (0.45), CSLA-CNT (0.62), EP-DFF-CNT (0.37), CNTT (0.42), OCG-CNTT (0.55), CNT-XOR (0.49), and the suggested 3D-CNTA (0.3) are the approaches with the lowest average power consumption. The findings for Noise (microvolts) for the identical technologies and CNT sizes are shown in Figure 4(b). SL-DFF (2.75), CNTFET (3.1), CSLA-CNT (4.2), EP-DFF-CNT (2.9), CNTT (3.05), OCG-CNTT (3.3), CNT-XOR (3.0), and 3D-CNTA (2.6) had the lowest average noise levels of the group. Due to its inventive design that maximizes the use of carbon nanotubes, the suggested 3D-CNTA regularly outperforms conventional approaches in terms of power consumption and noise levels. This demonstrates the promise of 3D-CNTA as an energy-efficient answer for future electronic applications.

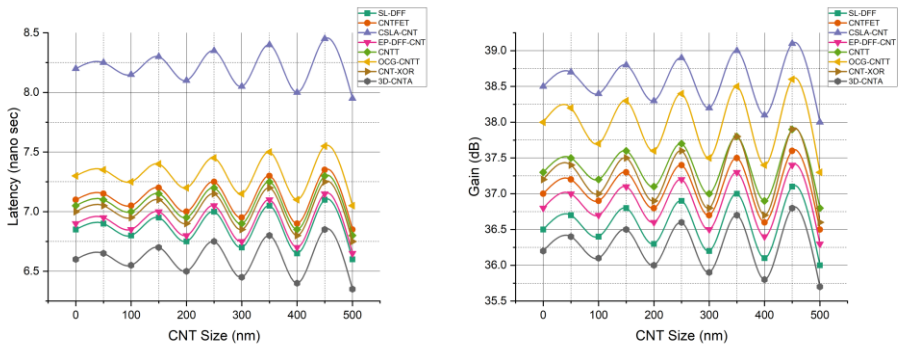

Figure 5(a): Latency analysis and Figure 5(b): Gain analysis

The findings for Latency (nanoseconds) for various CNT-based technologies at different CNT sizes are shown in Figure 5(a). SL-DFF (6.85), CNTFET (7.1), CSLA-CNT (8.2), EP-DFF-CNT (6.9), CNTT (7.05), OCG-CNTT (7.3), CNT-XOR (7.0), and 3D-CNTA (6.6) are the approaches that have the most prolonged latencies. The Gain (dB) findings for the identical technologies and CNT sizes are shown in Figure 5(b). SL-DFF (36.55), CNTFET (37.05), CSLA-CNT (38.55), EP-DFF-CNT (36.85), CNTT (37.35), OCG-CNTT (37.95), CNT-XOR (37.22), and 3D-CNTA (36.25) are the approaches with the highest average gain values. Due to its streamlined design, which reduces signal propagation time, the proposed 3D-CNTA beats previous methods in latency while retaining competitive gain levels.

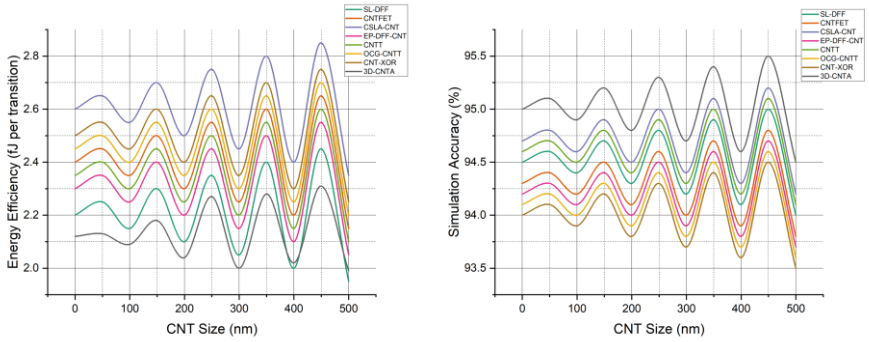

Figure 6(a): Energy efficiency analysis and Figure 6(b): Simulation accuracy analysis

The Energy Efficiency (femtojoules per transition) for various CNT-Based Technologies at different CNT sizes is shown in Figure 6(a). The following are the approaches' typical energy efficiency: CNTFET (2.4), CSLA-CNT (2.6), EP-DFF-CNT (2.3), CNTT (2.35), OCG-CNTT (2.45), CNT-XOR (2.5), and 3D-CNTA (2.12) are other examples of related structures. The Simulation Accuracy (%) for the identical technologies and CNT sizes is shown in Figure 6(b). The following result shows the typical simulation accuracy percentages for different techniques: CNTT (94.6%), OCG-CNTT (94.1%), CNT-XOR (94.0%), SL-DFF (94.5%), CNTFET (94.3%), CSLA-CNT (94.7%), EP-DFF-CNT (94.2%), CNTT (94.6%), and 3D-CNTA (95.0%). Due to its streamlined design, which reduces power consumption during transitions, the 3D-CNTA stands out for its remarkable energy efficiency. It features the best simulation accuracy, guaranteeing accurate electrical characteristic modeling. These encouraging results highlight the promise of the 3D-CNTA as a highly effective and dependable technology for the following electronic applications.

Power consumption (0.3 Watts), noise (2.6 microvolts), latency (6.6 nanoseconds), gain (36.25 dB), energy efficiency (2.13 femtojoules per transition), and simulation accuracy (95%) are only a few of the parameters that the proposed 3D-CNTA outperforms. Future electronic applications benefit from the high performance and low energy consumption of the proposed 3D-CNTA, which exceeds current approaches on several critical criteria.

Conclusion and Future Scope

This research emphasizes the crucial significance of transistors in modern electronics and underscores the growing need for enhanced speed capabilities to drive technological advancement. The introduction concisely outlines the vital importance of transistors and emphasizes the urgent need for innovative solutions to address present difficulties. The 3D-CNTA technology, distinguished by its complex three-dimensional arrangement of CNT, presents itself as a transformative approach. Significantly, comprehensive simulations continuously demonstrate the exceptional capabilities of 3D-CNTA compared to existing systems, suggesting significant gains in crucial parameters. The 3D-CNTA exhibits outstanding performance in several aspects, encompassing power consumption (0.3 Watts), noise (2.6 microvolts), delay (6.6 nanoseconds), gain (36.25 dB), energy efficiency (2.13 femtojoules per transition), and simulation accuracy (95%). The findings presented in this

study provide strong evidence that 3D-CNTA has the potential to alter the current state of electronic systems significantly.

However, it is crucial to acknowledge the pressing needs involved in expanding manufacturing methods and guaranteeing rigorous quality management for mass production. This study aims to analyze the future trajectory of overcoming these challenges to exploit the transformative potential of 3D-CNTA technology fully. This will lead to the emergence of a new era of high-speed, energy-efficient electronic devices, which have the potential to revolutionize multiple sectors within our technologically advanced society.

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