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Reconfigurable CMOS-LDO for with High PSRR at Low Quiescent Current

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Abstract

An integrated low-dropout (LDO) voltage regulator with low-noise, high power supply rejection ratio (PSRR), is proposed at 22 nm CMOS technology. The proposed regulator is able to produce an output voltage regulation at 1.8 Volt process, at low dropout voltage of 25 miliVolt on supply of the input voltage at 450mV. The features of LDO regulator are observed at high PSRR under the frequency bandwidth lies in 100 kHz and 1 MegaHertz. The LDO design also gives performance in terms of output noise performance below 350 nanoVrms/√Hertz at 100Hertz.

Keywords: *CMOS; regulation; power supply rejection ratio; low-dropout (LDO).*

1. INTRODUCTION

Architectures associated to System on Chip (SoC) scheme, often offering power management feature as the integrated function with the DBB, ABB & RF applications, presenting new challenges to the circuit system design experts, even for conventional and commonly used circuit architectures. As analog process with high-voltage technology replaced with highly dense, deep-submicron architecture based circuit designs, the units used under power management should be adaptable to circuit designs without the sacrifice of the design integrity. Challenges become more complicated as the tolerances specified by customers because of limitations of the processes under deep-submicron level are getting narrow.

The increasing demand for portable devices, the battery energy efficiency becoming most concerned problem. Hence, management of system of power supply is indispensable for consumer products of modern time. For system of power management, LDO regulator are most common part because of the characteristics, like simplicity, low noise, board space size & costing.

Traditional LDO regulators have compensation incorporated by employing an equivalent series resistor (ESR).When gain and pole positions fluctuate due to variations in load, this adjustment is hardly helpful [1-4]. Recently, there has been an increase in interest in high performance liner regulators for load management and high power supply rejection. Figure 1 illustrates the evolution of the SoC system, an LDO that is favored for lowering footprint size and cost. For consumer products of modern applications, high PSR performance and high precision are desired. LDOs having high DC gain characteristics helps in achieving such requirements. LDOs are presently used in DSPs device for achieving concerns of precision that has high load regulation and RF based circuits with high sensitivity to noise

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which requires high PSR. Latest design of LDOs do not have requirement of off-chip capacitor, hence it is suitable for SoC based applications and greatly reduces the cost [5]-[7].

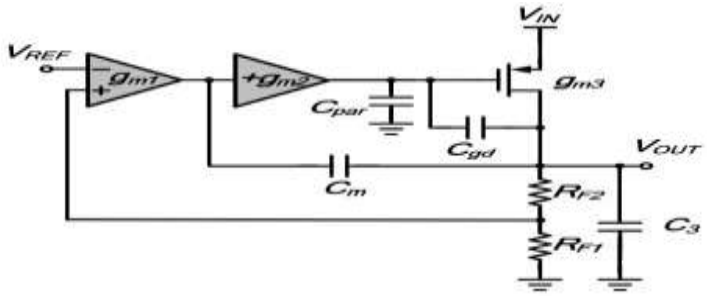

Figure 1. Conventional three-stage LDO regulator.

These days, low dropout voltage regulators use a high low-frequency gain to improve the load & line regulation and do so without the need of capacitors, which reduces the external side footprint area. The Miller compensation topology, which consists of a Miller capacitor and a capacitor of a power MOSFET device at gate-to-drain connection, is intrinsic to the three-stage LDO architecture. Nevertheless, minimum load constraint affects such topologies [8]–[12]. Unwanted oscillation is a concern when it is very lightly loaded. Therefore, minimum load restriction is a problem for Miller compensation topology based LDO devices [9, 10]. The complex pair that produces an output pole and a pole at the power MOSFET gate terminal when there is a light load is the cause of the system bandwidth limit. That is, a 90-degree design for the system phase margin is required [1, 5]. As a result, the limited bandwidth and improper phase margin cause the reaction time to slow down.

There are two distinct approaches for reducing the minimum limitation of load. One significant strategy to provide stability under light load is to shift the pole on output terminal port or using the power MOSFET gate terminal for a greater frequency. One way of regulating the damping factor and achieve the decrease for quality factor is via the use of the damping factor controller (DFC) methodology [5, 12]. The other DFC capacitor shorts the DFC amplifier to obtain a small resistance and provide a smaller time constant than that of the DFC amplifier without the short circuit created by the Miller capacitor. But because the capacitance C_{gd} affects the power MOSFET in the calculations, its minimal load current is not given sufficient consideration. At greater load current conditions, the complex poles become visible due to the presence of the large capacitance C_{gd}. When the load current drops, this approach still has the high-Q issue. With the same magnitude as the Miller capacitor, a DFC compensating capacitor can handle a load current range of around 100µA to 10mA. It implies that the system instability might be caused by the high quality factor issue. Consequently, to reduce the minimum load constraint, the Q-reduction methodology [1] employs a different method to move the pole at the power MOSFET gate terminal at a greater frequency. Approximately 100µA is the minimal load reduced by employing a 1pF compensating capacitor as the C_{cf}. Nonetheless, the extra compensating capacitor C_{cf} offers a ground channel to the gate terminal of the p-type power MOSFET, allowing noise from the supply voltage to pass straight through the output. This indicates that while the minimum load current issue is resolved, the PSR performance is significantly worsened [13]– [15]. Power supply rejection (PSR) is essential because low-dropout (LDO) regulators reject voltage source ripples. A large DC gain and bandwidth error amplifier is required for a traditional LDO regulator [16]. The circuit bandwidth of voltage regulators needs to be increased, and they also need to maintain a greater power supply rejection (PSR) in comparison to nearby blocks. Even at frequencies as high as 300 kHz, conventional LDO regulators offer poor PSR.A number of methods have been proposed to raise the PSRR. Enhancing the PSR can be achieved by utilizing two regulators or an RC filter at the LDO regulator output [17]. This method can raise the PSR, but because of the series resistor or second-stage regulator connection, it also raises the dropout voltage. Using

a charge pump and an NMOS pass transistor is an additional method [18]. Because an NMOS pass transistor is used in this approach, the supply voltage must be lower than the NMOS bias terminal. [18] put in place a charge pump to supply an independent regulator bias at a greater level. But this method adds complexity to the circuit and wastes more DC power.

A low-noise, high-PSRR integrated LDO is provided in this paper. At RF range, the LDO may drive chip loads either on or off. This article is motivated by many factors: presenting silicon data from a cutting-edge SoC application where the dc/dc switch mode power supply (SMPS) output is used for power in the linear regulator under LDO application for RF based devices; discussing and analyzing techniques and methods for low-noise, high-PSRR LDO design; and giving an overview of the limitations and capabilities of 22nm CMOS technology in relation to the direct-battery connect power management circuit design. The conventional LDO regulator architecture is given in Section 2. Section 3 describes circuit implementation of the proposed LDO regulator. Finally, a conclusion is made in Section 4.

2. Conventional LDO with moderate OpAmp gain:

Figure 2 depicts an LDO regulator used in a traditional circuit design application. It has an error amplifier to compare the feedback circuit voltage and Vref and a PMOS transistor as a pass element. Three routes make up the traditional LDO regulator's coupling mechanism for noise to the regulator's output. The first line is connected via the pass transistor, the second path is connected to the input supply voltage through the error amplifier, and the third way is connected to the V_{ref}. The resistors R_1 and R_2 on the first path mostly rely on the feedback network at low frequencies. The load capacitance (C_O), also known as the C load, begins to grow in frequency as it performs its tasks to eliminate input side ripples. The error amplifier's DC gain and bandwidth set a restriction on the second path PSRR. As a result, the error amplifier faces the need that its DC gain and bandwidth be sufficiently high. Due to capacitance at the pass transistor gate terminal, the second path effect is weak at high frequencies. The bandgap reference or the bias voltage source restrict the PSRR value in the third path. As the input-to-output voltage difference at which the LDO can no longer regulate against additional input voltage reduction, this is known as the dropout voltage ($V_{DROPOUT}$). The pass element functions as a resistor with a value equal to the drain-to-source on resistance (RDS_{ON}) in the dropout voltage zone. In terms of load current and RDS_{ON}, the dropout voltage is stated as follows:

$$V_{DROPOUT} = I_{LOAD} \times RDS_{ON} \quad (1)$$

RDS_{ON} including resistance from the pass element, on-chip interconnects, bond wires & leads may be estimated by the dropout voltage of LDO.

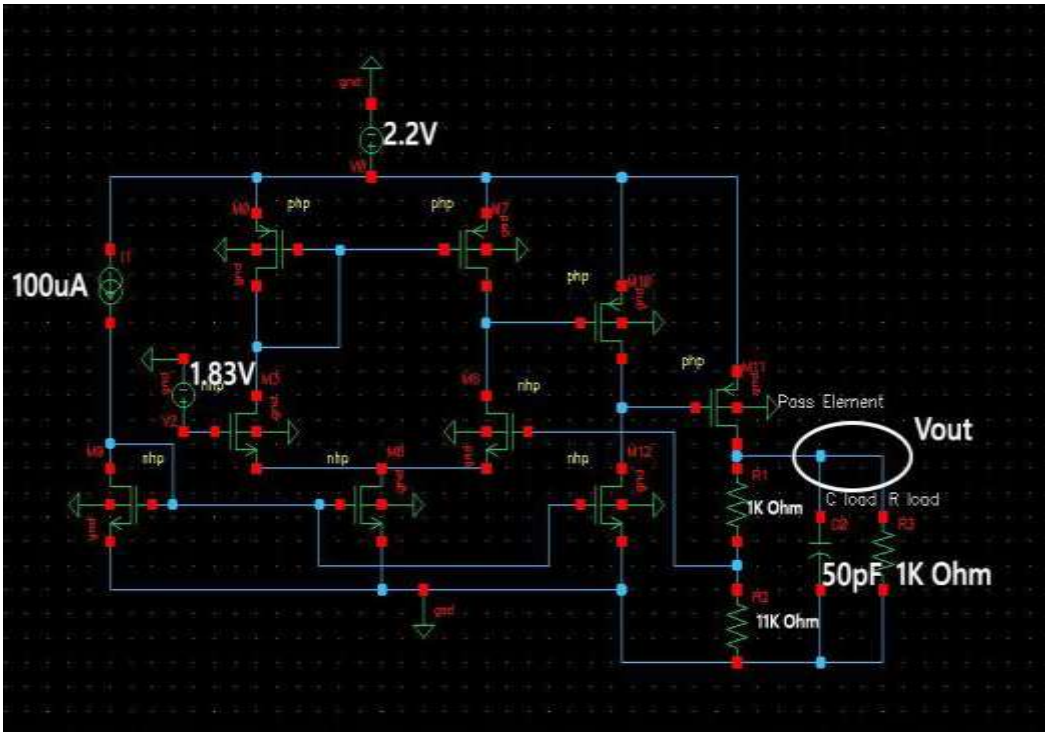

Figure 2: Full schematic LDO design used in conventional approach

Table 1: Results obtained for conventional LDO design shown in figure 2

1	Vo	0.88V	4	Bias Current	350 uA
2	Reference input (at opamp gain= 62dB)	1.83V	5	Avg. Power Dissipation	570 uWatt
3	PSRR	-58dB at DC	6	CMOS	22nm 2.3V process

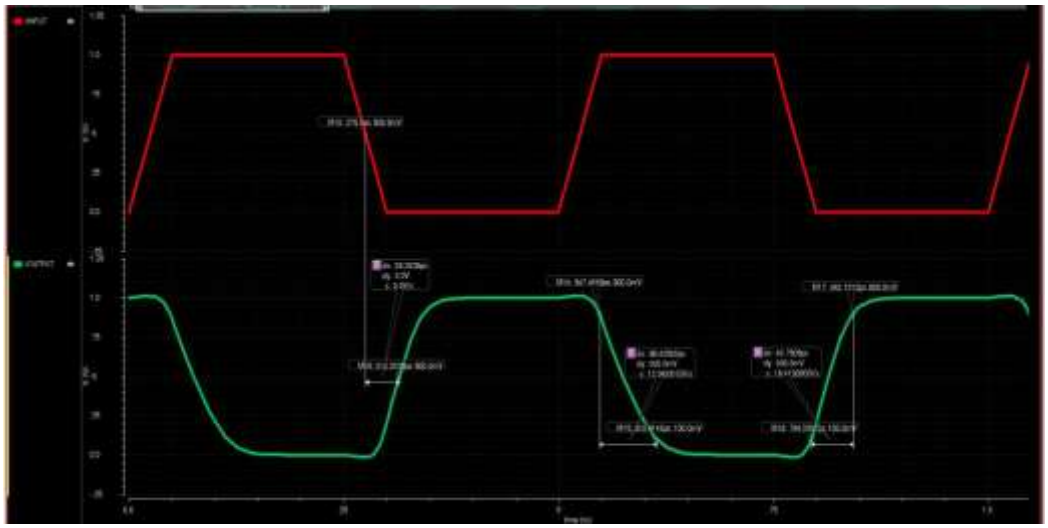

Figure 3: Output voltage drooping due to variation in load

Figure 3 is showing the output voltage for the conventional LDO design of figure 2.The i/p side voltage (top) waveform is shown in top while the output voltage is shown in bottom in this figure. The response of output voltage (bottom) is observed in the condition when the load is varying. The drooping in the output voltage may be observed due to the effect of variation of load. Hence the conventional design lacks the stability for load variation.

3. Proposed LDO voltage regulator design:

The particular opamp design used here is in fully differential mode using common mode feedback (CMFB) technique, due to which it is capable of giving moderate to high gain in a single stage. In table 2 the citcuit parameters for the improved LDO design are provided for fully differential mode opamp design. The MOSFET parameters are defined in terms of W/L ratio.

	Table 2: Circuit design parameter for proposed LDO regulator design shown in figure 4.				
	Device id	W/L ratio		Device id	W/L ratio
1	M_{10}=M_{13}	4micro/2micro	4	M_{2A}=M_{2B}	1micro/2micro
2	M_{11}=M_{14}	12.8micro/800n	5	M_{1A}=M_{1B}	8micro/600n
3	M_{12} =M_{15}	2micro/800n	6	C_O	50pf

In this paper an improved LDO design is shown in figure 4.In this proposed design the voltage source has connection with MOSFET M_{12} and M_{15} and the I_{Bias} terminal is given to MOSFET M_{1A} and M_{1B}.The output terminal is at the junction of CMOS pair of M_{14} and M_{15} (OUT).V_{IN}^- and V_{IN}^+ signals are provided at M_{1A} and M_{1B}.M_{2A} and M_{2B} are connected to ground and both are complementary MOSFETs of M_{1A} and M_{1B}.Voltage divider circuit is given in between common point of M_{1A}-M_{1B} and M_{2A}-M_{2B} CMOS pair. The fully differential mode circuit shown in figure 4 is used as the high gain error amplifier stage of proposed LDO circuit design having input connected to resistor R1 and R2 as shown in figure 4.

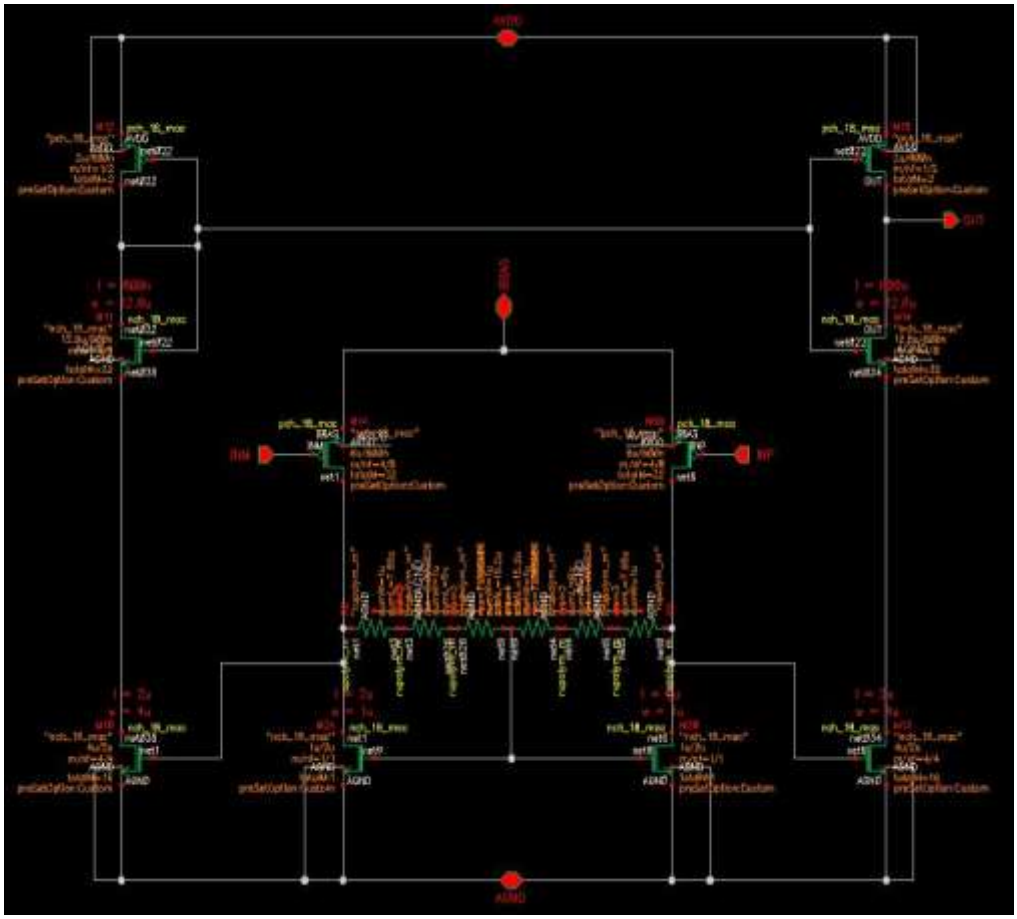

Figure 4: High Gain Opamp frequency response, used in the design

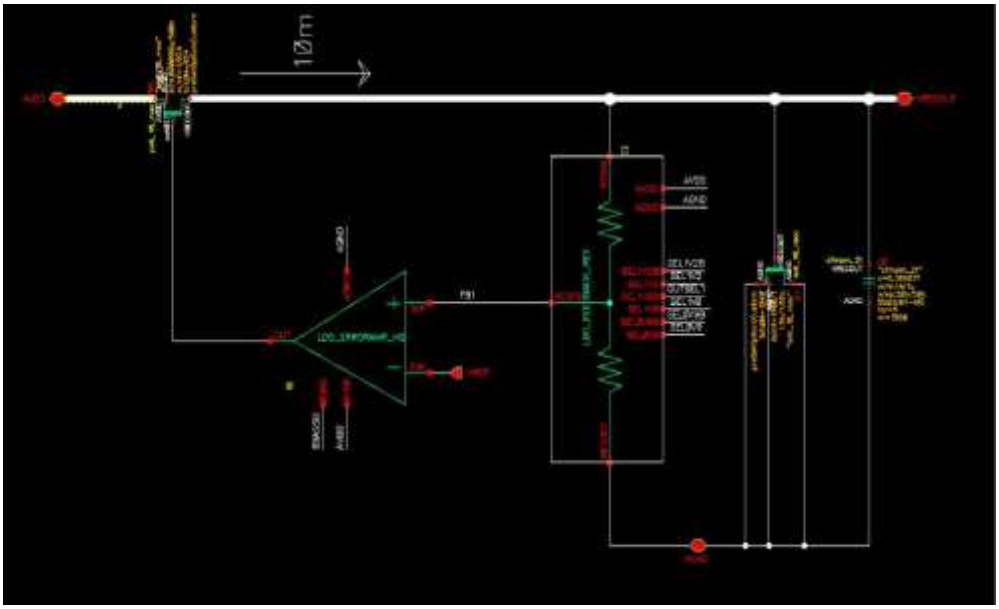

Figure 5: Schematic design of improved LDO voltage regulator

	Table 3: Target Specifications for improvised LDO design shown in figure 5.				
1	I/P voltage	0.75-0.9 V	6	Load Regulation:	0.33 V/A
2	Max. op Current	200mA at 0.9V	7	PSRR:	-110dB
3	Reference input	1.2V	8	Bias Current:	200 uA
4	Line Regulation:	9.5 mV/V (or 0.0095)	9	Avg. Power Dissipation:	360 uWatt
5	CMOS	22nm 1.8V process	10	Op voltage	0.85V

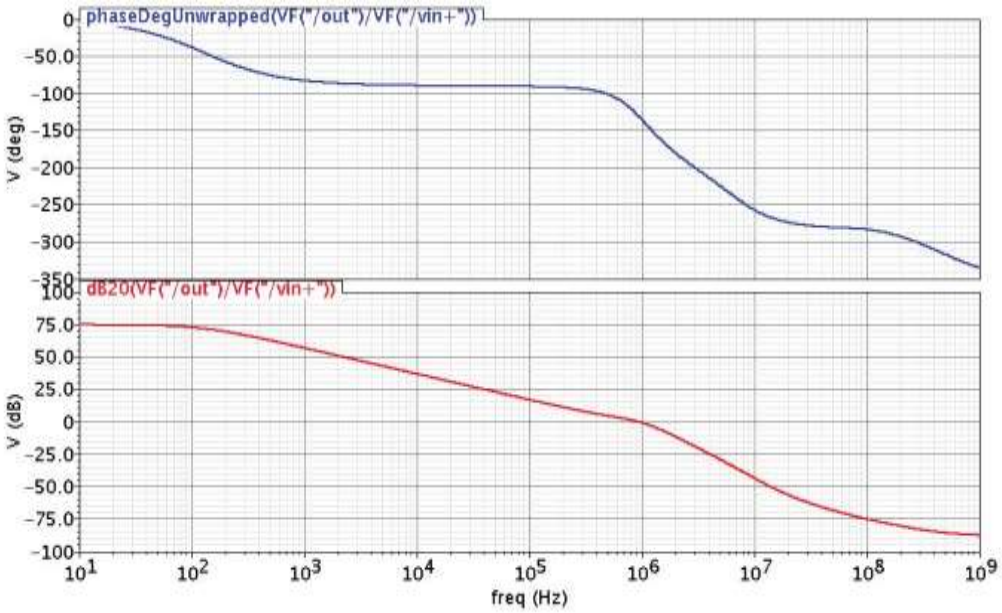

Figure 6: Op-amp gain frequency response (76 dB)

Line regulation definition and explanation

Line regulation defined as measure of the ability of a regulator circuit for maintaining a specific value of output voltage with respect to variation in the i/p side supply voltage. Line regulation are expressed as:

Line Regulation = $\Delta V_o / \Delta V_i$ (2)

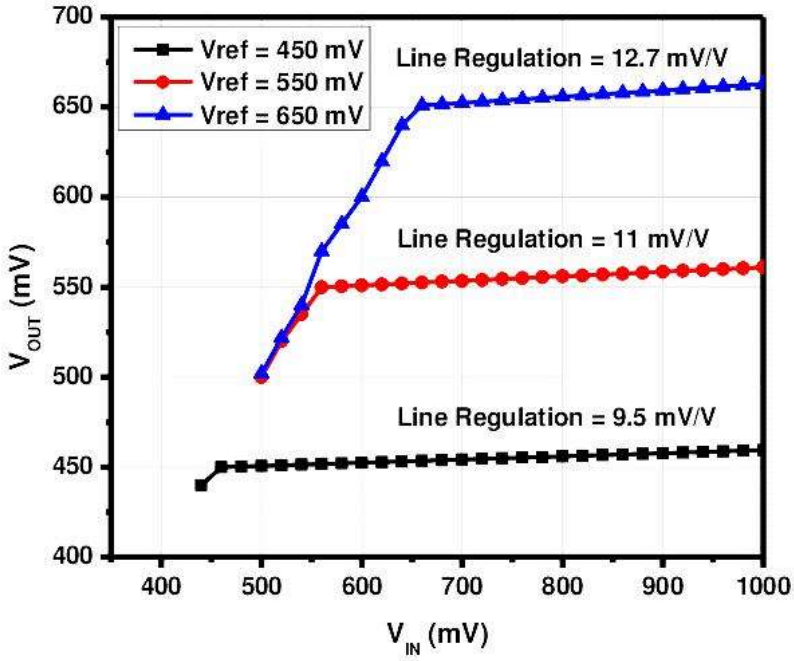

Figure 7: variation in O/P side supply Voltage with respect to the changes in I/P Voltages

Load regulation definition and explanation: It is defined as the measurement of the ability of a regulator circuit as a device to maintain the specific value of output voltage with respect to variation in conditions of load. Expression of load regulation is given as:

Line Regulation = $\Delta V_o / \Delta I_L$

	Table 4: Line regulation evaluation parameters for proposed LDO regulator.	
	OP current (mA)	OP voltage (V)
1	30	0.998
2	60	0.989
3	90	0.985
4	120	0.978
5	150	0.956

Power Supply Rejection Ratio: The power supply rejection ratio, or PSRR for short, measures how well an LDO regulator circuit can avert regulated output voltage fluctuations brought on by changes in input voltage. It is sometimes referred to as ripple rejection. Similar equation for line regulation is applicable to PSRR with only exception that in this case the consideration coves all the frequency spectrum. PSRR is expressed as:

Ripple Rejection:

$$PSRR = \frac{V_{o,\,ripple}}{V_{i,ripple}} \text{ at all frequencies}$$

When a linear regulator is powered by the output of a dc/dc switch mode power supply (SMPS), the PSRR in the frequency range of 100 kHz to 1 MHz is highly important. This frequency bandwidth is below the SMPS output ripple.

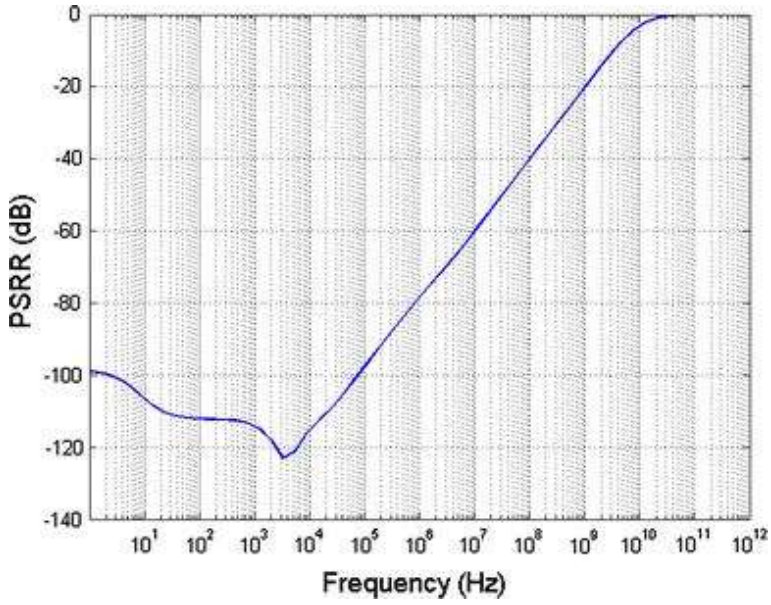

Figure 8: Achieved PSRR response of the proposed design (PSRR = -110dB at low freq/DC)

The control loop is generally has the dominant contribution in maintaining PSRR. A large value capacitor at output, is added alongwith the bypass capacitors for in improving PSRR performance.

4. Conclusions

A LDO regulator with enhanced PSRR is proposed using the CMFB scheme in 22 nm CMOS technology. The amplifier, introduced a high gain frequency response for achieving an optimum ripple cancellation response. Proposed LD voltage regulator is useful in providing -110 dB of PSRR at low frequency DC. The LDO design is giving a dropout voltage of 9.5mV/V at a 450V input. It can also provide 425 to 450 mV at a range of 450–900 mV of the voltage as input. Load regulation performance observed to be 0.33 (mV/mA). The circuit is consuming 200 mA at an input supply voltage of 0.9 V.

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