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Improving Low Energy Technology Application Performance: Enhancing Low Noise Amplifier via Stabilization and Input-Output Component Matching Design

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Abstract

The increasing miniaturization, enhanced integration, and improved accessibility of technology have led to the widespread adoption of complementary metal-oxide-semiconductor (CMOS) technology in wireless applications. In recent years, the utilization of wireless technology has experienced significant proliferation, encompassing not just consumer electronics but also extending to medical applications such as the deployment of body temperature and heart rate monitors. The recent emergence of a novel practice in swiftly monitoring information through the utilization of portable and wireless devices has incorporated the use of low noise amplifiers as a means of achieving energy efficiency. The objectives pursued in the proposed research article include doing an analysis of current trends in low-noise amplifier (LNA) needs and designs through a comprehensive review of existing literature. Additionally, the research aims to determine the optimal LNA topology and specifications for a certain frequency band or spectrum of application.

Keywords: *LNA, stabilization, I/O matching, low energy technology.*

1. Introduction

The increasing prevalence of wireless standards and the emergence of dynamic standards and applications, such as software-defined radio, are fueling the need for the forthcoming generation of wireless devices. These devices aim to integrate several standards within a single chip-set, thereby enabling a diverse array of services. The desirability of reconfigurable multi-standard portable devices is evident, as it allows for the efficient sharing and reuse of hardware components, hence effectively reducing both device costs and physical footprint. This study proposes several advanced circuit topologies that are suitable for multi-standard applications and capable of meeting various standards at a reduced cost. The focus of this research paper proposal will be on the following significant aspects:

1. Broad difficulties facing contemporary RF/Wireless systems and corresponding resolutions

2. Design considerations and obstacles encountered in the development of RF-CMOS Integrated Circuits

3. The topics of interest in this discussion are Low Noise Amplifiers (LNA) and Radio Frequency Mixers (RF-Mixer).

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In order to achieve reduced power consumption in wireless RF systems, such as RF-Mixed-Signal System-On-Chip systems, it is imperative to possess a comprehensive comprehension of low-power design across several levels, including components, circuit blocks, sub-systems (e.g., receiver, transmitter, and PLL), and system levels. The primary focus of this study is the optimization of power consumption for wireless RF integrated circuit (IC) circuits.

Reducing the cost of the localization function poses a significant challenge for wireless sensor nodes equipped with wireless localization capabilities. It is imperative to minimize the cost of each wireless sensor node due to the substantial quantity often required for various applications. The utilization of a standard CMOS technology is advantageous in terms of cost reduction, since it is particularly well-suited for efficient large-scale manufacturing processes. The implementation of a systematic strategy and comprehensive design can also result in a reduction in the expenses associated with a certain system. Implementing a streamlined and pragmatic system architecture has the potential to reduce expenses and minimize energy usage.

RF Receiver Chain and LNA Design Aspects

Following the Low Noise Amplifier (LNA) stage, a down-conversion mixer is employed to convert the incoming Radio Frequency (RF) signal to the intermediate frequency (IF), as illustrated in Figure 1. The IF is characterized by a lower frequency compared to the original RF signal. In the direct conversion design, the frequency of the IF stage commences from the direct current (DC) level. The utilization of separate frequencies in the IF stage facilitates the attainment of essential high gain and high stability in RF receivers, as it effectively isolates the RF stage from the IF stage.

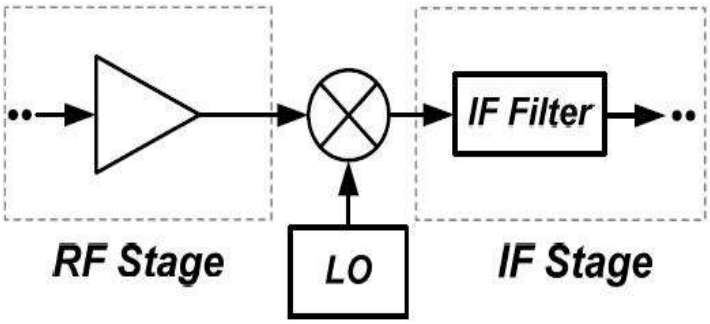


Figure 1: Block diagram of a mixer in RF architecture consisting LNA and mixer

The initial stage of the front-end receiver circuit for Bluetooth Low Energy (BLE) is the low noise amplifier (LNA). The design of a Low-Noise Amplifier (LNA) consists of five components: geographies, input matching organizations, source degeneration critique circuits, biasing circuits, and result matching organizations. The circuit was fabricated using the 45 nm processing technique derived from the generic processing design kit (GPDK). To ensure proper construction of a Low-Noise Amplifier (LNA), it is important to possess a comprehensive understanding of performance characteristics and the underlying principles of RLC circuit theory.

The advanced degrees of integration in modern integrated circuit (IC) technologies enable the incorporation of supplementary passive components, such as inductors, onto a single chip. This capability facilitates the attainment of the objectives associated with efficient radio frequency (RF) complementary metal-oxide-semiconductor (CMOS) technology. Moreover, the utilization of advanced design technologies incorporating smaller device sizes mitigates the adverse impact of transmission line effects, which were more pronounced in earlier technologies. These features facilitate the resolution of challenges associated with the integration of direct conversion receivers into a single integrated circuit. The limited adoption of this architecture can be attributed to four primary factors:

The following concepts will be discussed in an academic manner:

- I/Q mismatch
- DC offsets
- Flicker noise
- Even order distortion

Radio frequency integrated circuits (RFICs) are the essential elements that constitute portable wireless communication devices. CMOS technology is widely regarded as a highly effective technological solution for the implementation of RF front-ends. The viability of this is supported by several key properties, including cost-effectiveness, consistent device scalability, and high levels of integration. The move towards the 5GHz band for operating frequency is occurring due to a rise in customer demand for electronic services. This suggests that there is a need for the implementation of innovative RF front-end designs.

The Low-Noise Amplifier (LNA) holds significant importance in a conventional design as it plays a crucial role in determining the overall sensitivity of the system. Therefore, it is imperative that the system meets several performance restrictions. The input impedance should remain constant at 50 ohms, the noise figure should be minimized, and the gain of other stages should be increased to effectively suppress noise.

MOSTs biased in the weak/moderate inversion region are commonly employed to attain a reduced level of thermal noise. Additionally, chopper stabilization techniques are utilized to relocate 1/f-noise from the signal band, hence ensuring a favorable overall noise performance.

2. Literature Survey

The study conducted by Chang et al. (2020) [10] this paper presents the design and implementation of a low-power CMOS low noise amplifier (LNA) working at a frequency range of 17.7-42.9 GHz. The proposed LNA is intended for radio cosmic applications and is implemented using a 65-nm CMOS technology. Based on several approaches for data transmission upgrades, the proposed Low Noise Amplifier (LNA) exhibits a significant noise figure and a substantial gain enhancement across a broad frequency range, all while consuming minimal power. The LNA, or Linear Needs Assessment, is a valuable instrument that can facilitate the attainment of one's objectives. Within the frequency range of 17.7 to 42.9 GHz, the data transmission capacity at the 3-dB level exhibits a peak rise of 20.1 dB. Additionally, the noise figure (NF) falls within the range of 2.8 to 4.3 dB. Operating at a frequency of 28 gigahertz, this particular approach demonstrates a power consumption of less than 18 milliwatts of direct current (dc) power, while exhibiting an output power at the 1 dB compression point (OP1dB) of 2.2 decibels milliwatts (dBm). The study emphasizes the significance of distributed K-band and Ka-band low-noise amplifiers (LNAs) by presenting a figure-of-merit (FOM) value of 19 GHz/mW. The total surface area of the chip, inclusive of padding, measures 0.45 mm2.

The study conducted by Amgothu Laxmi Divya et al. (2020) [11] presented a comprehensive investigation on the design and implementation of a low noise amplifier for a collector RF front-end used in narrowband distant communications. The LNA serves as the focal structure square for the distant collector. A cascode CMOS LNA is specifically developed for reconfigurable applications such as Wireless LAN. The primary objective of this document is to outline a strategy for conducting a Low Noise Amplifier (LNA) fitting specifically designed for remote applications, while also emphasizing the need for more precise execution measures. The objectives of this project involve utilizing an inductive degeneration normal source stage in order to get sound reduction and significant amplification. The suggested Low Noise Amplifier (LNA) encompasses the complete

reenactment process, leading to a recurrence band of 2.44GHz. However, the optimal information and result coordinating organization is achieved by effective reverse shielding and excellent security measures.

The body drifting and self-inclination approach was introduced by Chang et al. (2021) [12]. In this technique, the relationship between the semiconductor's body and its channel is established through an opposition, which in this particular study is set at 13.6 k. The methodology for sub-6 GHz 5G systems is addressed by a low-power 3-9 GHz CMOS low-noise amplifier (LNA). The improvement in the S21 and noise figure (NF) of the low-noise amplifier (LNA) can be attributed to the forward body-to-source inclination (VBS), such as the minimal edge voltage Vth, and the liberation of semiconductors from substrate leakage. The designers assert that these CMOS LNAs have exceptionally low power levels, which are some of the lowest ever recorded for data transmission beyond 6 GHz and a noise figure (NF) below 3.5 dB.

The authors of the study exhibit the phenomena of body drifting and self-inclination within a 3-9 GHz CMOS low-noise amplifier (LNA). The improvement in the LNA's S21 and NF can be attributed to the implementation of forward-one-sided voltage biasing (VBS), namely through the use of small threshold voltage (Vth), as well as the liberation of semiconductors from substrate spillage. The achievement of low power dissipation (PD) is attributed to the utilization of low supply voltages (VDD) of 1 V or 0.8 V, which is significant in light of the low threshold voltage (Vth). The well-established performance of the Low Noise Amplifier (LNA) offered by the LNA proves its appropriateness for use in 5G networks that operate at frequencies lower than 6 GHz. This is evident from its notable figures, such as a Noise Figure (NF) of 2.89 dB at a Power Density (PD) of 3.3 mW.

In a study conducted by Sakshi Singh Dangi et al. (2021) [13], the authors designed a Radio Frequency Integrated Circuit (RFIC) using Complementary Metal Oxide Semiconductor (CMOS) technology. In addition to Bluetooth, Worldwide Interoperability for Microwave Access (Wi-MAX), and Wireless Fidelity Local Area Network (Wi-Fi LAN), CMOS technology is increasingly being adopted in the corporate sector. The utilization of Complementary Metal Oxide Semiconductor (CMOS) technology for the construction of Radio Frequency Integrated Circuits (RFICs) presents notable benefits in terms of both speed and cost. Moreover, CMOS technology enables a higher level of miniaturization on a single integrated circuit. At its fundamental essence, CMOS is conceptualized in this manner. The utilization of this technique is prevalent in the field of very large scale integration (VLSI), wherein a multitude of semiconductors can be effectively integrated into a single chip or substrate. RF designers derive enhanced benefits from the expeditious operational efficacy of CMOS technology. The remarkable levels of coordination on a single chip facilitate the effective operation of CMOS technology within the gigahertz frequency range, resulting in abundant performance while maintaining a cheap cost. The decision to adopt CMOS technology is straightforward in light of the current landscape of virtual broadcast communications and the demand for high flagging rates inside the predominant segment of the radio frequency.

3. Methodology

The objective is to integrate many standards into a unified chip-set with the aim of reducing power consumption, optimizing space utilization, and enhancing the competitive advantage of the resultant product. Figure 3 presents the frequency spectrum for multiple standards. Based on the available evidence, it is possible to infer two distinct conclusions.

- The definitions of "signal power" and "frequency bands" vary across different standards.

- Numerous channels have the potential to access the collector with minimal pre-separation, so functioning as in-band obstacles and causing significant distortion.

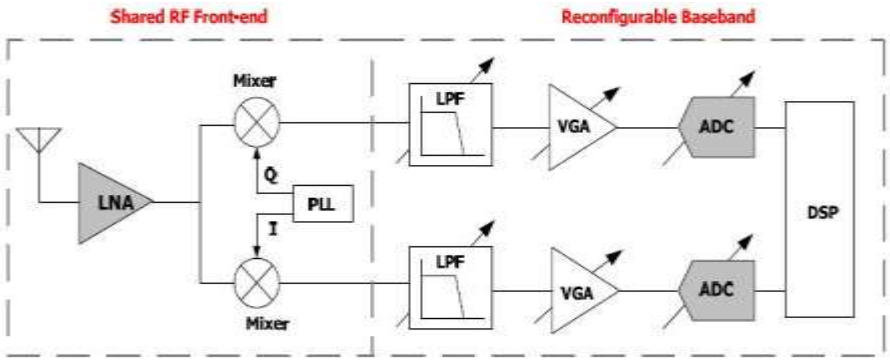


Figure 2. A down-conversion MIXER-based reconfigurable direct conversion receiver is depicted as a block diagram.

Based on the provided data, it is possible to identify two significant challenges associated with the design of RF-Down-conversion mixers.

Prior to delving into the analysis of various radio receiver architectures, it is essential to provide an early explanation of some specific challenges associated with these structures. In the realm of wireless communication, a multitude of users share a finite number of frequency spectrum frequencies. Therefore, it is possible for strong signals to coexist with weak signals in close vicinity. In order to achieve effective signal reception and interference rejection, an RFIC radio receiver must include active and passive components that may possess inherent imperfections. The receiver design is characterized by two primary concerns:

- The repudiation of visual representations
- The concept of range of motion refers to the extent to which a joint or series of joints can move in various directions.

The recipient must possess the capability to discern and choose the desired signal amidst the multitude of other signals present within the spectrum. In an optimal situation, the achievement of this objective can be facilitated by employing a bandpass filter characterized by a channel-width bandwidth and a center frequency aligned with the desired RF signal.

The key determinants of a receiver's dynamic range encompass the noise figure, the nonlinearity of the low-noise amplifier (LNA), and the first mixer. In scenarios when the desired radio frequency (RF) signal exhibits low strength and is accompanied by robust interfering signals, the efficacy of the preselection RF band pass filter in attenuating undesired signals is compromised. The presence of these large interferers has the potential to overpower the subsequent intermediate frequency (IF) circuits, so hindering the proper processing of the desired signal after it has been amplified in the receiver's front-end components, such as the low noise amplifier (LNA) and mixer. Furthermore, these notable sources of interference introduce distortions to the signal-to-noise ratio (SNR) of the receiver, hence increasing the level of input referred noise.

Moreover, the presence of nonlinearities in the Low-Noise Amplifier (LNA) and mixer might result in the occurrence of intermodulation distortions from these strong interfering signals, which may subsequently affect the desired channel during the down conversion process. Due to the inability of the IF filter to discern between undesired signals and the essential IF signal, these distortions exhibit characteristics akin to noise.

One plausible argument could involve outlining a professional and technical approach to attaining the specified objectives, which will be further elaborated upon in subsequent

sections. Figure 3 illustrates the wireless receiver architecture employed for reconfigurable direct conversion, as presented in the preceding section.

The primary design of the work, namely the low-noise amplifier (LNA) circuit, can be achieved by employing parallel narrowband receiver paths with band selection switches. Nevertheless, this approach is characterized by higher costs, increased spatial requirements, and more power consumption. A versatile and cost-efficient solution for minimizing silicon size and power consumption is the utilization of a highly linear broadband RF front-end equipped with interchangeable baseband blocks. This approach enables the system to meet diverse needs while minimizing the need for extensive hardware implementation.

There exist a multitude of circuit designs that necessitate simulation and analysis in order to reach a targeted design with desired low power consumption and high operational speed attributes. To accomplish the objective, it will be necessary to utilize a robust Circuit simulator program. Below is a compilation of several tools that fall under this category.

Simulator environment: SPICE (schematic level)

• The HFSS and SPICE software, developed by Keysight Technologies as part of their Advance Design System

Adoption of technology nodes:

• CMOS (Level 49 and above) (Level 49 and above)

• Either 130 or 180 nm (Low voltage node)

The planned research project aims to follow the following objectives:

- By a literature review, current trends and analyses on LNA requirements and designs will be examined.
- Establishing the LNA's final topology and requirements for the application's chosen band (spectrum).
- Finalizing the schematic topology according on the application and technology (RF-CMOS here at 65 or 130 nm).
- Planning and modelling the performance of the LNA in a real RF environment.
- Verification and adjustment of the design to meet the specifications. (Publishing the conventional and original findings found in credible journals).
- The topic of discussion pertains to CMOS technology, specifically focusing on its application and relevance for individuals at or above Level 49.
- The low voltage node options for the semiconductor technology are either 130 nm or 180 nm.

The proposed research project seeks to pursue the subsequent objectives:

- This study aims to conduct a literature research to analyze current trends and requirements in the field of low-noise amplifiers (LNAs).
- The final topology and specifications for the application's chosen band (spectrum) of the LNA are determined.
- The schematic topology will be determined according on the specific application and technology requirements, such as RF-CMOS at either 65 or 130 nm.
- The task at hand involves the strategic planning and meticulous modeling of the Low Noise Amplifier (LNA) within an authentic Radio Frequency (RF) setting.

• The process of verifying and adjusting the design to align with the specified requirements. Disseminating the established and novel discoveries documented in reputable scholarly publications.

4. Results and Discussion

Amplifier with stabilization components added

In order to enhance the performance of the amplifier and mitigate the presence of offset and flicker noise, a chopper technique is employed. The primary purpose of a ripple reduction loop (RRL) is to mitigate the effects of ripple resulting from the up-modulation of offset and flicker noise. The elimination of the notch in the overall transfer function of the RRL operation occurs when a multi-path architecture is utilized, incorporating both a low-frequency path (LFP) and a high-frequency path (HFP). The implementation of the low frequency path amplifier involves the utilization of the Regenerative Receiver with Limiter (RRL) and the chopper technique. The utilization of a class-AB output stage in the high-frequency route amplifier is employed to enhance power efficiency. The system demonstrates a frequency response of first-order as a result of the transfer functions of the low-frequency path (LFP) and high-frequency path (HFP), which are effectively compensated for by the implementation of layered Miller compensation. The low-noise multi-path amplifier was fabricated using a 0.18 m 1P6M complementary metal-oxide-semiconductor (CMOS) technology. The suggested low-noise functional amplifier has an operational area of 1.18 square millimeters and a power consumption of 0.174 milliwatts, operating at a voltage of 1.8 volts. The proposed low-noise amplifier exhibits an input referred noise level of 11.8 nV/Hz, a unit gain bandwidth (UGBW) of 3.16 MHz, and a noise efficiency factor (NEF) of 4.46.

The external source impedance has been configured to a value of 50 Ohms, and a matching network has been connected to the input. Therefore, assuming that the input matching network remains constant, the conjugate of S22 can be identified as the ideal load reflection coefficient.

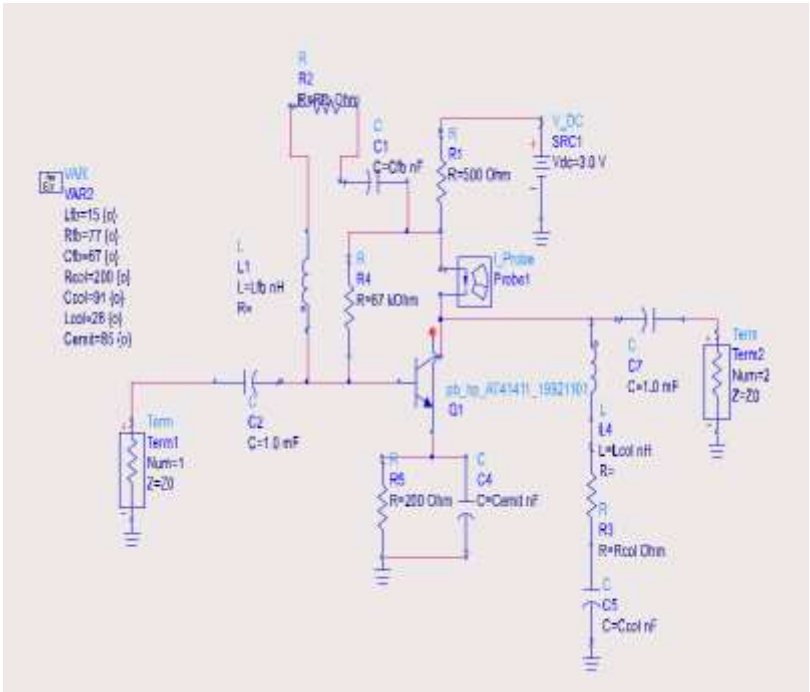


Figure 3: Amplifier with stabilization components

Figure 4: Frequency response of amplifier gain

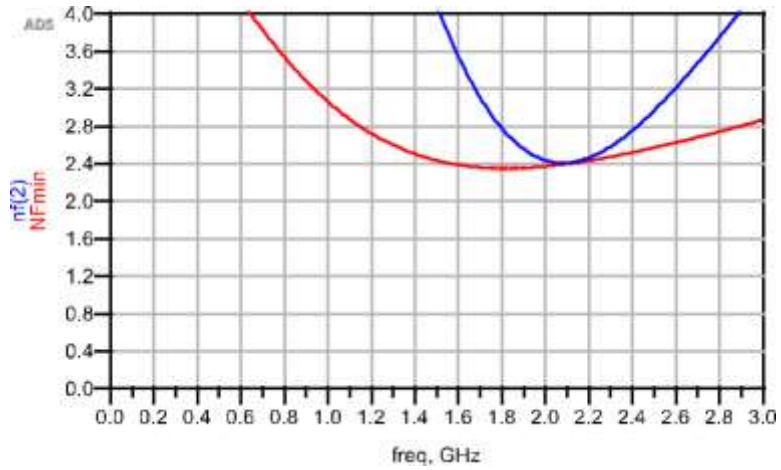
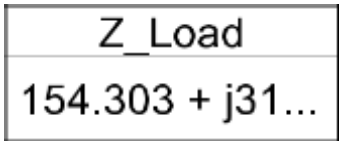


Figure 5: Noise efficiency factor response



Optimization of amplifier input and output matching networks for gain,input match, output match, and noisefigure.

Previous studies have presented many LNA circuits implemented in RF CMOS technology. However, the existing literature lacks comprehensive design methodologies specifically tailored for achieving extremely low noise values. In numerous scenarios where the prioritization of linearity outweighs the significance of noise figure, there exists a compromise between linearity and noise figure, resulting in a partial sacrifice of the latter. However, it is possible to achieve robust linearity and noise performance, which will be discussed in further depth in subsequent sections of this study. The optimization of noise performance in receivers mostly revolves around setting gain and power dissipation, as the LNA (Low-Noise Amplifier) significantly influences the overall noise figure. During the interim period, the remaining characteristics are customized to meet the specific needs of the various applications they serve, utilizing interactive and simulation techniques.

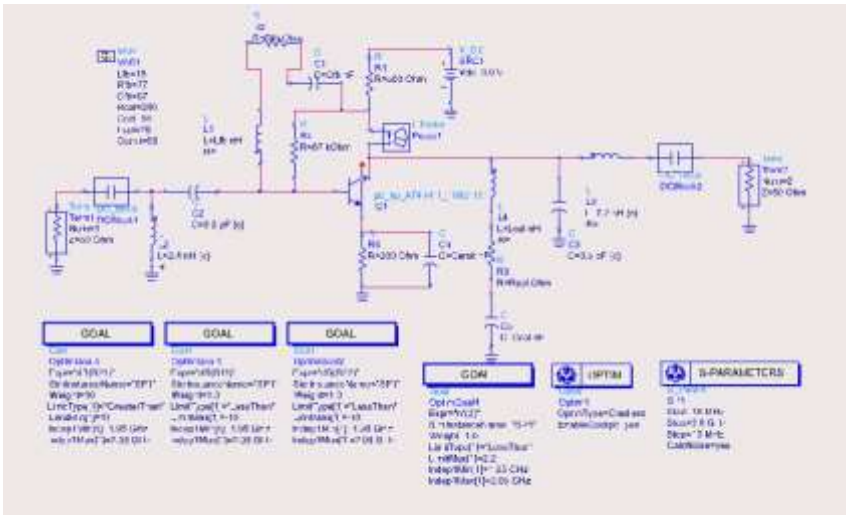


Figure 6: Amplifier with input and output matching networks

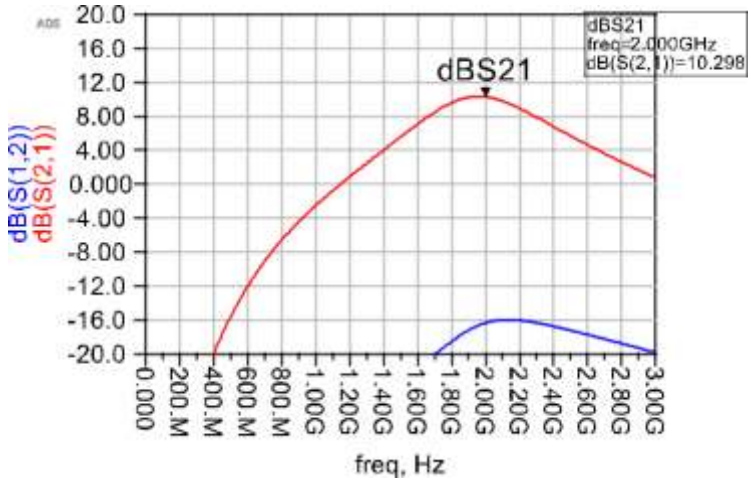


Figure 7: Frequency response of Amplifier with input and output matching networks

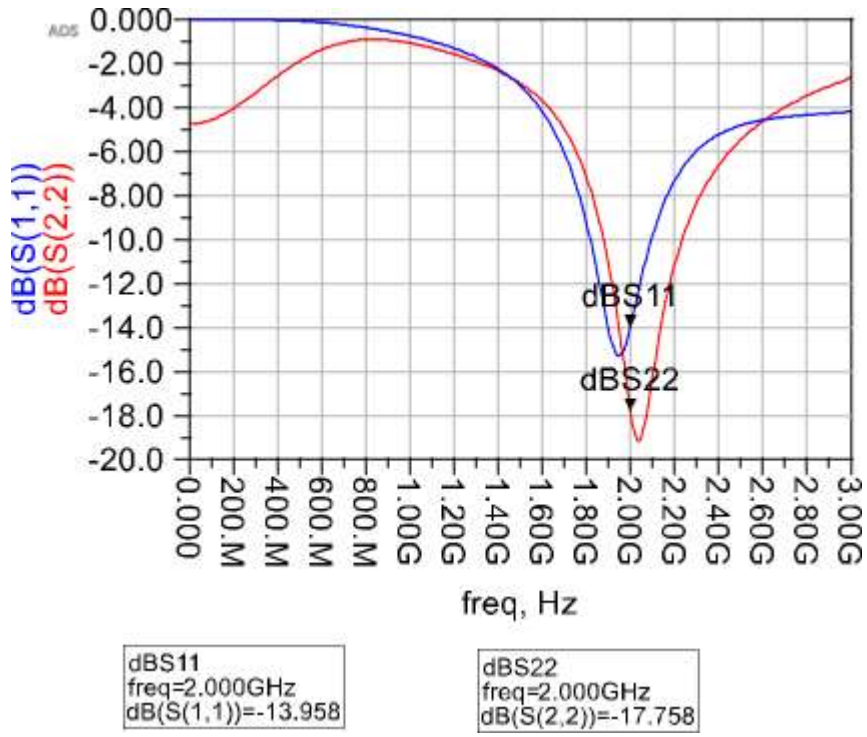


Fig 8: Amplifier with stabilization, input, and output matching components added

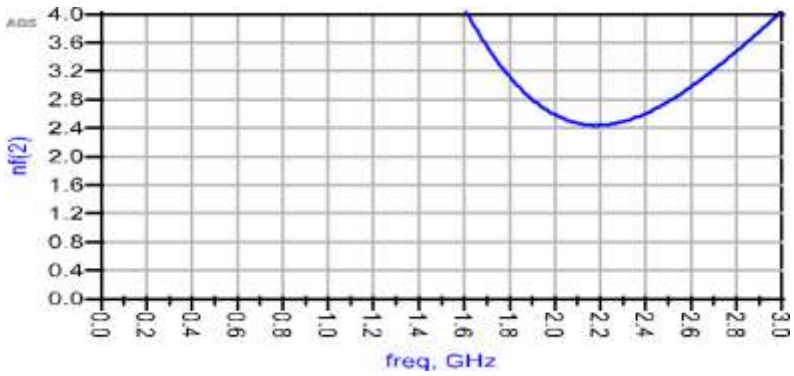


Figure 9: Noise efficiency factor response of Amplifier with input and output matching networks

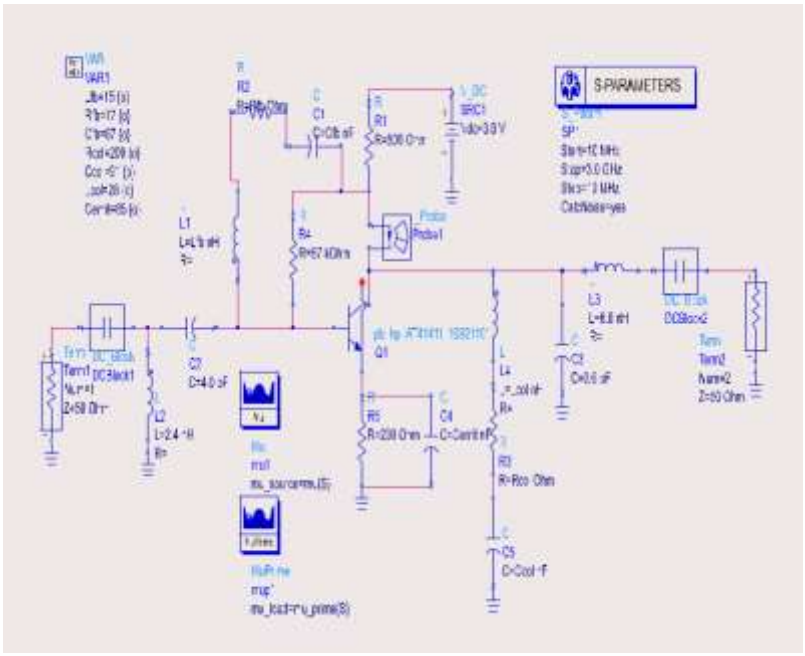


Figure 10: Amplifier with stabilization, input, and output matching components added

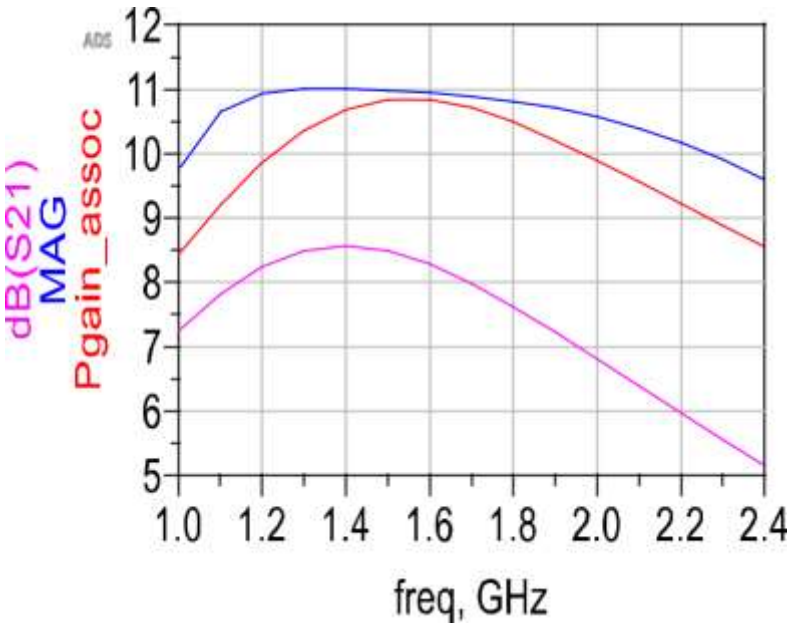


Figure 11: Frequency response of amplifier with stabilization, input, and output matching components added

The parameters of interest include the maximum achievable gain, the equivalent power gain when the input and output are conjugately matched for minimum noise figure, and the value of dB (S21). The utilization of Z0 Ohm terminations enables the determination of the minimal noise figure, expressed in decibels (dB), as well as the noise figure.

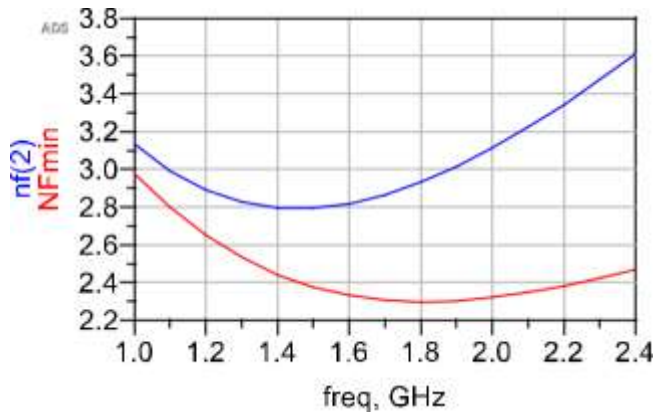


Figure 12: Noise efficiency factor response of amplifier with stabilization, input, and output matching components added

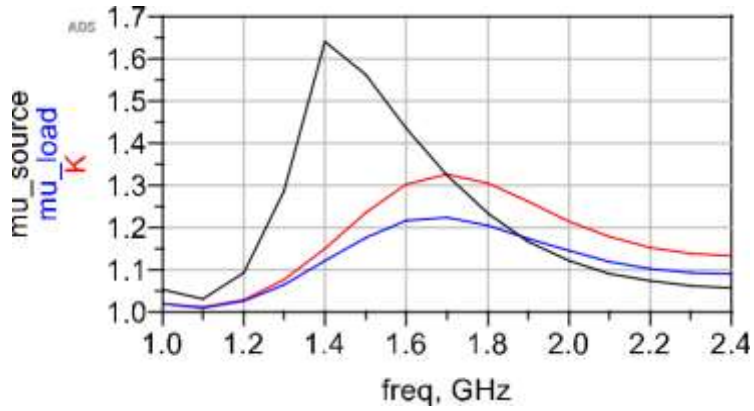


Figure 13: Stability Factor, K Geometric stability factor smu_source and mu_load

5. Conclusion:

SiGe (BiCMOS) and CMOS transistors are widely employed in the construction of low-noise amplifiers (LNAs), as evidenced by the prevalence of these technologies in research articles. Nevertheless, the GaAs-pHEMT is commonly employed in the construction of most commercial Low Noise Amplifiers (LNAs). Moreover, it is worth noting that a limited number of commercially available Low Noise Amplifiers (LNAs) have a noise figure that is below 0.5 dB. The silicon process has a greater degree of integration compared to alternative transistor technologies. Until recently, the RF market has been predominantly controlled by the GaAs-HEMT and other BiCMOS technologies, particularly those utilizing SiGe, owing to their exceptional performance. Nevertheless, the CMOS technique is currently gaining prominence. The trade-off between noise figure, linearity, gain, and power can be observed. By making certain concessions in terms of power, gain, and various other factors, it is feasible to achieve a system that exhibits a low noise figure and favorable linearity characteristics. The requirements of an LNA design are determined by the function or application for which it is utilized. In many instances, base stations prioritize the attainment of low noise figure (NF) and favorable linearity characteristics. However, WLAN, Bluetooth, GPS, and certain other applications place greater emphasis on linearity and a noise figure that is deemed satisfactory.

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